International Workshop on Gate Insulator 2003
November 6-7, 2003
Miraican Hall, National Museum of Emerging Science and Innovation
Tokyo, Japan

Thursday, November 6		
10:00 Registration Start		
10:30-11:05 Welcome and Plenary Session		
Chairpersons: A. Morino/Selete, T. Arikado/Selete		
10:30	Opening Remark	A. Morino/Selete
10:40	Keynote Speech	T. Nishitani/NEC
11:05-12:15 High-k 1		
Chairperson: A. Toriumi/Univ.of Tokyo		
11:05	*Invited Speech:* Hf-based High-k Dielectrics	J. C. Lee/Univ. of Texas
11:40	*Invited Speech:* Implementation of High-k Gate Dielectrics - a Status Update	S.De Gendt/IMEC
12:15-13:30 Lunch		
13:30-15:00	Poster Session	
HK-1	Degradation of Dielectric Characteristics of Underlying Ultrathin SiO_2 Films by Al Adsorption in High Vacuum	K. Yamabe/Univ. of Tsukuba
HK-2	The Influence of Silicon Nitride Cap on NBTI and Fermi Pinning in HfO_2 Gate Stacks	T. Sasaki/Selete
HK-3	Vapor-Liquid Hybrid Deposition (VALID) of Hafnium Silicate Films Using $Hf(OtC_4H_9)_4$ and $Si(OC_2H_5)_4$ Precursors	Y. Xuan/MIRAI
HK-4	Electrical Characteristics of Rare-Earth Oxide Stacked-Layer Structures	S. Ohmi/Tokyo Inst. of Technology
HK-5	Effects of Hf Sources, Oxidizing Agents, and NH_3 Radicals on Properties of HfAlOx Films Prepared by Atomic Layer Deposition	T. Kawahara/Selete
HK-6	Charge State Dependent Point Defect in High-k Dielectric HfO_2	K. Shiraishi/Univ. of Tsukuba
HK-7	Solution-Based Fabrication of High-k Gate Dielectrics	Y. Aoki/RIKEN
HK-8	Improvement in the Uniformity and the Thermal Stability of Hf-silicate Gate Dielectric by Plasma-Nitridation	S. Kamiyama/Selete
HK-9	Gate Dielectrics on Strained-Ge Layers on $Si_{1-x}Ge_x$/Si Virtual Substrates	S. Bhattacharya/The Queen's Univ. of Belfast, UK
TO-1	Method of Increasing Gate Nitridation and its Impact on CMOS Devices	V. P. Gopinath/LSI Logic
TO-2	Nitrogen-Related Enhanced Reliability Degradation in nMOSFETs with 1.6nm Gate Dielectric	C.-H. Chien/NNDL, Taiwan
TO-3	Ultra-Thin SiN Gate Dielectric Fabricated by N_2 Plasma Direct Nitridation	M. Inoue/Renesas
FE-1	Effects of Interaction between HfO_2 and Poly-Si on MOSCAP and MESFET Electrical Behavior	V. S. Kaushik/International SEMATECH/IMEC
FE-2	Improved Performance of FETs with HfAlOx Gate Dielectrics Using Optimized Poly-SiGe Gate Electrodes	A. Muto/Selete
RE-1	Self-Organized Si Suboxide (SiOx,x<2) Interfacial Layers-Optimization of Performance and Reliability in Advanced Devices	G. Lucovsky/NCSU
RE-2	Impacts of Hole Trapping on the NBTI Degradation and Recovery in PMOS Devices	H.-C. Lin/NNDL, Taiwan
MO-1	Resonant Tunneling in Stacked Dielectrics: a Novel Approach for Obtaining the Electron Tunneling Mass-Conduction Band Offset Energy Products for Advanced Gate Dielectrics	G. Lucovsky/NCSU

MO-2	Proposal of Quantum Well Gate Insulating (QWGI) Structures for Band Offset Engineering from First-Principles Calculations	Tatsuo Shimizu/Toshiba
ME-1	Ru Gate Electrode for a La-oxide Gate Insulator Deposited by Metalorganic Chemical Vapor Deposition	Takashi Shimizu/AIST
ME-2	A Study on the Vth Shift of HfAlOx MISFETs with n+/p+ Poly-Si and TiN Gate Electrodes Fabricated by Replacement Gate Process	Y. Akasaka/Selete
ME-3	Energy Barrier Heights of Ultra-thin Silicon Dioxide Films with Different Metal Gates	N. Yoshii/Osaka Univ.
OA-1	Properties of Tantalum Silicate Thin Films Prepared by Metalorganic Decomposition	K.M.A. Salam/Muroran Inst. of Technology
15:00-16:15 High-k 2		
Chairperson: T. Yasuda/AIST		
15:00	*Invited Speech:* Atomic Layer Deposition Chemistry, Mechanisms and Related Physical Properties of High Permittivity Dielectric Oxides	K. Kukli/Univ. of Helsinki
15:35	Separate and Independent Control of Interfacial Band Alignments and Dielectric Constants in Complex Rare-Earth/Transition Metal (Re/Tm) Oxide	G. Locovsky/NCSU
15:55	Study of Defects in MOS Structure Using HfAlOx Gate Dielectric by Means of Positron Annihilation	A. Uedono/Univ. of Tsukuba
16:15-16:30 Break		
16:30-18:00 High-k/FET		
Chairperson: T. Mogami/NEC		
16:30	*Invited Speech:* Gate Dielectric Scaling for High-Performance CMOS: from SiO_2 to High-k	R. Chau/Intel
17:05	*Invited Speech:* Electrical and Physical Properties of Poly-Si Gated HfSiON Gate Dielectrics	H. Niimi/Texas Instruments
17:40	*Invited Speech:* HfSiON Gate Dielectrics for CMOS Applications	M. Takayanagi/Toshiba
18:00-20:00 Reception		

Friday, November 7		
9:30 Registration Start		
10:00-11:50 Thin SiON		
Chairpersons: S. Kimura/Hitachi, H. Watanabe/NEC		
10:00	*Invited Speech:* Extending the Life of N/O Stack Gate Dielectric with Gate Electrode Engineering	Q. Xiang/AMD
10:35	*Invited Speech:* Advanced Oxynitride Gate Dielectrics for CMOS Applications	J. Yugami/Renesas
11:10	Drastically Improved NBTI Lifetime by Periodic Plasma Nitridation for 90nm Mobile Applications at Low Voltage Operation	T. Kawae/Tohoku Univ.
11:30	Improvement in Thermal Stability of the Interfacial Layer for Poly-Si/HfAlOx Gate Stacks	R. Mitsuhashi/Selete
11:50-13:20 Lunch		
13:20-14:35 Modeling: Carrier Mobility		
Chairperson: S. Takagi/AIST, Univ. of Tokyo		
13:20	*Invited Speech:* Reduced Electron Mobility in High-k MOSFETs Due to Insulator Optical Phonons: Density, Temperature and Material Dependence	M. V. Fischetti/IBM

13:55	Comparative Study of Carrier Mobility and Threshold Voltage between N- and P-MOSFETs in TaN Gate CMOS with EOT=1.5-2nm HfAlOx	H. Ota/MIRAI
14:15	Dependence of Electron Mobility by Remote Coulomb Scattering on Dielectric Constant Distribution in Stacked Gate Dielectrics	M. Ono/Toshiba
14:35-14:45 Break		
14:45-16:20 High-k 3		
Chairperson: K. Shiraishi/Univ. of Tsukuba, Y. Akasaka/Selete		
14:45	*Invited Speech:* EOT Scaling and Device Issues for High-k Gate Dielectrics	M. I. Gardner/International SEMATECH/AMD
15:20	In-situ HfSiON/SiO_2 Gate Dielectric Fabrication Using Hot Wall Batch System	T. Aoyama/Selete
15:40	Effects of Nitrogen Incorporation into HfAlOx Films on Gate Leakage Current - From XPS Study of Hf Bonding States	T. Nishimura/MIRAI
16:00	Further EOT Scaling of Ge/HfO_2 over Si/HfO_2 Systems	K. Kita/Univ. of Tokyo
16:20-16:30 Break		
16:30-18:30 Panel Discussion: Development Strategy of Gate Dielectrics: Ultra-thin Oxynitride versus High-k Materials		
Organizers	H. Iwai/Tokyo Inst. of Technology	
	M. Hiratani/Hitachi, T. I. Tech.	
	M. Takayanagi/Toshiba	
	H. Kitajima/Selete	
Moderator	H. Iwai/Tokyo Inst. of Technology	
Panelists	Ho-Kyu Kang/Samsung	
	T. Horikawa/AIST(MIRAI)	
	K. Torii/Selete	
	Y. Tsunashima/Toshiba	
	J. Yugami/Renesas	
	S. De Gendt/IMEC	
	H. Niimi/Texas Instruments	
	M. V. Fischetti/IBM	
	R. Chau/Intel	
18:30-18:35 Closing Remark		
18:30	Closing Remark	F. Ootsuka/Selete